Top Skills

FPGA
Embedded Systems
PCB design

Languages

Italian (Native or Bilingual)
English (Elementary)

Embedded System HW Engineer

Summary

I’m a hardware engineer with 20 years relevant experience in embedded systems design.
In the last 8 years I worked at Ericsson SpA telecom industry implementing complex mixed signal PBA in indoor radio bridges for the backhaul of mobile networks, mainly designing, developing and debugging dual microprocessor control & communication chipsets of the traffic node boards also supporting FPGA, FW and Layout designers.
In the past I worked about 1 year at Vega srl home-building automation company mainly designing,developing and debugging lift control systems based on Microchip microcontroller from concept to production.
At the beginning of my career I worked for about 5 years at SIGMA SpA company as FPGA\HW\FW egineer designing, developing and debugging mainly embedded systems with DSP & FPGA for self-service and payroll machine.
The international working environment (team distributed in different parts of the world America-Asia-Europe), especially over the past 8 years, has allowed me a comparison during the development stages both of different methodologies and different cultures, leading necessarily to exploit and develop the qualities as flexibility and adaptation’s capacity. In addition, cross-functional team-working during development with a large group of different disciplines and deployed in different areas has allowed me to increase the ability of organization and task priority.

Experience

Balance Systems Corp

Hardware Engineer
2015 - Present (9 years)
Pessano con Bornago, Lombardy, Italy

HW\FPGA Designer:

• Design, development, schematic-entry of Analog\Digital Embedded Systems;
• PCB Layout Support;
• Analog Frontend Spiece and PCB SI Pre-Layout and Post-Layout Simulations;
• FW support for BSP \ Boot development;
• FPGA development;
• Development of specific tests and support scripts for the Basic Unit Test;
• Basic Unit Test of the electronic board.

Exprivia Telco and Media

Embedded System HW Engineer
April 2014 - January 2015 (10 months)

- Design, development and verification of microprocessor\microcontroller chipsets in telco embedded systems (for internal proects).
• Design, development, schematic-entry of Digital Embedded Systems;
• PCB Layout Support;
• SI Pre-Layout and Post-Layout Simulations;
• FW support for BSP \ Boot development;
• Development of specific tests and support scripts for the Basic Unit Test;
• Basic Unit Test of the electronic board.
- PCB SI Simulator in Python (Python course internal proect).

Devoteam auSystems SpA

9 years 3 months

Senior HW Designer consultant @ emmedidue srl
August 2013 - March 2014 (8 months)

Embedded Systems HW Consultant.

Design, development and verification of microprocessor\microcontroller chipsets in telco embedded systems.

Projects:
1) Design and development of electronic actuator monitor board for Electromechanical Actuator in avionic systems.
2) Design and development of communication RS485\RS422 "switch" board for Electromechanical Actuator in avionic systems.

Activity and responsibilities:

o Writing the Design Specification;
o Components evaluation and selection;
o Schematic Entry implementation;
o Layout constraints implementation and support to PCB layout team.

HW Designer consultant @ Ericsson SpA
March 2006 - July 2013 (7 years 5 months)

Projects:

1) Design, development and verification of digital chipset of a Switch Ethernet Board to support PDH & Ethernet traffic in a rack-based Traffic Node (NPU1D).
2) Design, development and verification of digital control&traffic chipset of a stand-alone “Low Cost” Switch Ethernet Modem Board for the PDH & Ethernet Traffic Node (CN510R2).
3) Design, development and verification of digital control&traffic chipset of a Switch Ethernet board prototype to verify HW\FW platform’s performace and evaluate if it can be used as reference platform for “master unit” functionality in a rack-based Traffic Node System (NPU1x FUM).
4) Design, development and verification of digital control&traffic chipset of a stand-alone Modem Board for the PDH & Ethernet Traffic Node (CN510R1).
5) Design, development and verification of digital control&traffic chipset of an “agile” stand-alone\rack-based Modem Board for the PDH Traffic Node (CS).
6) Verification of an Altera StratixII’s FPGA that implement XPIC functionality (Cross Polar Interference Cancellation) in the Modem board for Basic Traffic Node.
7) Design, development and verification of an ATM Switching Board for the Minilink Traffic Node (rack-based system) supporting IMA function on ATM group (AAU).

Activity and responsibilities:

o Writing the Design Specification;
o Schematic Entry implementation;
o Layout constraints implementation and support to PCB layout team;
o Pre-Layout and Post-Layout simulation
o Writing the Verification Strategy and Verification Specification;
o Testbench implementation and board verification;
o CLI test scripts implementation to support board verification;
o Boot and BSP firmware team support;
o Verification report of the test results.

Hardware Designer consultant @ Ericsson SpA

January 2005 - February 2006 (1 year 2 months)

Projects:

1) Redesign HW of the XDB Switch Board for AXE Platform in order to meet the RoHS directives (XDB DfE).

Activity and responsibilities:

o Schematic Entry implementation;
o Layout constraints implementation and support to PCB layout team.
o Writing Verification Strategy and Verification Specification;
o Testbench implementation and board verification;
o CLI test scripts implementation to support board verification;
o Script Machine scripts implementation for automatic board verifcation ;
o Verification report of the test results.

VEGA srl

Senior Hardware Designer

September 2003 - December 2004 (1 year 4 months)

Projects:

1) Design and development of Elevator Control System Board (master board and slave boards) for Simplex/Multiplex Building Elevator system architecture.
2) Design and development of Embedded System Board for battery/virus recognition with CCD and Led technology in medical applications.

Activity and responsibilities:

o Writing System Requirements and Design Specification with customer support;
o Embedded systems architecture and schematic design;
o PCB layout design (2\4 layer boards);
o Analog front-end PSpice simulation;
o Board manufacturing management and component selection;
o FW design for Embedded systems;
o Writing Verification Strategy and Verification Specification;
o Testbench implementation and board verification;
o Verification report of the test results;
o Team leader for the Embedded Systems Test team;
o Team leader for the Embedded Systems Maintenance team.

Sigma SpA

Senior Hardware Designer

July 1999 - July 2003 (4 years 1 month)

Projects:

1) Project ”CASSA_2000”: paytoll self service machine for superhighway.

2) Project ”ECP500”: pipe controller self service machine for Post-Office.

3) Project ”ATM2000”: bancomat machine for banks.

4) Project ”AEROCASH”: bancomat machine for banknote remote pneumatic distribution from the caveau banks.

5) Project ”COINBASKET”: coin recognition equipment with electromagnetic sensors.

6) Project ”ETF500” and ”ETF2000”: self service machines for ticket railway payment.

Activity and responsibilities:

o Writing Design Specification;

o Board architecture design and schematic development;

o FPGA and CPLD design;

o PCB layout design (4 layer boards);

o Analog front-end PSpice simulation;

o Board manufacturing management and component selection;

o FW design for Embedded systems verification (C\Assembly code HAL Layer);

o Writing Verification Strategy and Verification Specification;

o Testbench implementation and board verification;

o Verification report of the test results;

o Manufacturing test-bench design and support.

EUROMECC sas

Electromechanical worker

May 1998 - June 1999 (1 year 2 months)

Production & Maintenance of the Energy Generator.

Activity and responsibilities:

o Implemetation of electrical and mechanical assembly of energy generator

SIGMA SpA

FPGA Hardware Designer

September 1996 - April 1997 (8 months)

University Stage Project: ”Banknote Acceptor”.

Banknote recognition equipment with CCD image sensor.

Activity and responsibilities:

o Board architecture design and schematic development;

o FPGA architecture design and schematic entry development;

o Writing Verification Strategy and Verification Specification;

o Testbench implementation and board verification;

o FW verification team support;

o Verification report of the test results.

Education

Università Politecnica delle Marche

Electronic Engineering, Automation · (1992 - 1997)

I.T.I.S. “G. Montani” – Fermo (AP)

High school Engineer, Industrial Electronic · (1988 - 1992)